



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,064	02/12/2002	Antonio Asaro	00100.00.0130	6702
23418 7590 01/16/2007 VEDDER PRICE KAUFMAN & KAMMHOLZ 222 N. LASALLE STREET CHICAGO, IL 60601			EXAMINER MYERS, PAUL R	
			ART UNIT 2111	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE 3 MONTHS			MAIL DATE 01/16/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/074,064	Applicant(s) ASARO ET AL.	
	Examiner Paul R. Myers	Art Unit 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 November 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-31 and 33-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-28 and 33-35 is/are rejected.
- 7) ☐ Claim(s) 29-31 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 11/13/06 have been fully considered but they are not persuasive.

In regards to applicants argument that “the claim is not selectively screening out or letting through certain bits in a data value”: the claim language states “wherein the register configuration logic configures the at least one register flop to be read and or writable based on at least one mask value stored in the memory”. This claim language makes clear that the mask value is used to screen out or let through (i.e. read and/or write) certain bits in a data value. A mask bit makes the data value accessible and the only possible accesses to a memory are read and/or write.

In regards to applicants argument regarding the combination of Gillespie and Surugucchi et al: Gillespie teaches the ROM storing initial configuration information. Gillespie however does not expressly state that this configuration information would include initial base addresses and mask values. The examiner recognizes that the configuration information should include such information as initial base addresses and mask values. However, since Gillespie is silent upon the form of the configuration information, the references to Venkat and Surugucchi et al which teach that configuration information would include initial base addresses and initial mask values respectively were cited.

In regards to applicants argument that “Surugucchi et al. explicitly teach that the BASS control logic unit updates the registers in the second configuration register space (which includes the BASS 1 memory mask) with the values in the first configuration space when the values in the

Art Unit: 2111

first configuration space are set and/or modified.”: First Surugucchi et al was cited solely for the teaching that mask values are included as part of configuration information. Second Applicants own invention updates the mask values from the ROM (which is flash writable see Page 1 lines 17-18) into the BAR.

In regards to applicants argument that applicant can find no mention of a data bridge having read only memory storing mask values: Gillespie teaches a data bridge having a ROM storing initial configuration information. Venkat teaches storing the initial base addresses as part of the configuration information of the devices.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 4-11, 13, 15-17, 19, 22-23, 25-28, 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillespie et al PN 5,859,987 in view of Surugucchi et al PN 6,094,699 and Venkat PN 5,857,083.

In regards to claims 1, 8, 10-11, 19, 28, 34, 35: Gillespie et al teaches a data bridge system, comprising: an interface (interface to primary PCI bus 9 or alternatively interface to local memory bus 11) for transferring data; a plurality of application-specific integrated circuits (ASICs) (21 and 23); a data bridge operatively coupled to each of the interface and the plurality of ASICs (7). Gillespie et al also teaches the bridge accessing a ROM storing configuration (31

Art Unit: 2111

Column 1 lines 59-65). Gillespie et al does not expressly teach the data bridge read only memory storing at least initial values and mask values for each ASIC of the plurality of ASICS. The examiner notes Gillespie et al does teach the bridge having a plurality of Base address registers in accordance with the AGP and PCI specifications, which would inherently need to be configured. Surugucchi et al teaches a bridge (210 or alternatively 210 and 212 taken together) including a mask register storing mask values for masking Base address registers in accordance with the attached peripherals. It would have been obvious to store the configuration mask values in the data bridge ROM of Gillespie et al because this would have consolidated configuration. Venkat teaches storing the initial base addresses in the configuration space of the devices. It would have been obvious to store the initial values in the configuration space of the combination of Gillespie et al in view of Surugucchi et al because this would have consolidated necessary configuration data.

In regards to claims 4, 22: Gillespie et al teaches the bridge having Base address registers. (part of the PCI specification incorporated in Gillespie)

In regards to claims 5-6, 13, 16, 23, 26: Gillespie et al teaches multiple base address registers in accordance with the PCI specification incorporated by reference in Gillespie et al. The PCI specification notes the number of Base address registers in a bus bridge is 6.

In regards to claims 7, 15, 25: Gillespie et al teaches multiple base address registers in accordance with the PCI specification which teaches the base address registers having

Art Unit: 2111

prefetchable and non-prefetchable and I/O space and non I/O space determinations. PCI specification page 196.

In regards to claims 9, 17: Gillespie et al teaches a configuration EEPROM. Which is an electrically erasable programmable ROM.

In regards to claim 27: Gillespie et al does not teach the EEPROM being removable. MPEP 2144.04 V C states to make separable is not a patentable distinction.

4. Claims 2-3, 12, 14, 18, 20-21, 24, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillespie et al PN 5,859,987 in view of Surugucchi et al PN 6,094,699 and Venkat PN 5,857,083 as applied to claim 1 above, and further in view of Applicants admitted prior art.

In regards to claims 2, 14, 18, 20, 24, 33: Gillespie et al does not teach the ASICs being graphics processors. Applicants admitted prior art teaches graphics processors (1020) attaches to a bus. It would have been obvious to include graphics processors because this would have allowed for the efficient control of graphics/video.

In regards to claims 3, 12, 21: Gillespie et al in view of Surugucchi et al and Venkat teach the bridge attached to a AGP bus described above. Gillespie et al in view of Surugucchi et al and Venkat do not teach a north bridge. Applicants admitted prior art teaches a north bridge

Art Unit: 2111

attaches an AGP bus. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use the bridge of Gillespie et al in view of Suruguchi et al and Venkat in the system of Applicants admitted prior art because this would have separated the graphics from the PCI system thus freeing the PCI system.

Allowable Subject Matter

5. Claims 29-31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In regards to claims 29-31: The examiner was unable to find the exact structure claimed.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

Art Unit: 2111


however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PRM
December 27, 2006


PAUL R. MYERS
PRIMARY EXAMINER